High-Efficiency Harmonic-Control Amplifier

Bernhard Ingruber, *Student Member, IEEE,* Werner Pritzl, *Member, IEEE,* Dieter Smely, Martin Wachutka, *Student Member, IEEE,* and Gottfried Magerl, *Member, IEEE*

***Abstract*—A half-sinusoidally driven class-A harmonic-control amplifier (hHCA) combines the advantage of high gain of class A with the advantage of high drain efficiency of class F. Consequently, power-added efficiency is increased as compared with state-of-the-art high-efficiency amplification techniques. As this innovative amplifier concept consists of a pulse-forming class-B amplifier stage followed by a class-A power-amplifier stage, intermodulation distortion is low even in saturation. The realization of such a two-stage hHCA offers 71% overall efficiency, 27.9-dBm output power, and 22.4-dB gain at 1.62 GHz. Two-tone measurements at 1-dB-gain compression, where the amplifier's single-carrier (SC) overall efficiency is still 64%, has demonstrated third- and fifth-order intermodulation distortion of −29 and −21 dBc, respectively.**

***Index Terms*—Class F, efficiency, harmonic control, linearity, microwave, power amplifier.**

I. Introduction

THE improvement of power-added efficiency and reliability of microwave power amplifiers has been investigated by many researchers over the last 25 years (see Table I). Most practical realizations of high-efficiency microwave power amplifiers make use of the so-called class-F mode, where the device is biased at class B or class B near class AB, and harmonics are controlled in such a way that the device output voltage becomes rectangular [1]–[5] (see Fig. 1). Many modifications of this switched-type amplifier have been introduced by several designers to improve the efficiency, e.g., class E [6], rectangularly driven class B (rB) [7], [8], or harmonic-reaction amplifier (HRA) [9], [10]. All of them operate at a class B near input level, where up to half of the input power is lost. This affects the gain, which is about 3 to 6 dB less than the corresponding class-A gain and, therefore, the power-added efficiency is drastically decreased as compared with the high device efficiency. Furthermore, device reliability is limited due to high negative gate-to-source voltage [11].

In this paper, we present an innovative amplifier concept which combines the advantage of high gain of class A with the advantages of high drain efficiency and low intermodulation distortion of class F [12].

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B. Ingruber, D. Smely, M. Wachutka, and G. Magerl are with the Department of Communications and Radio Frequency Engineering, Vienna University of Technology, A-1040 Vienna, Austria.

W. Pritzl is with the R&D Department of ELB-Form GmbH, A-1040 Vienna, Austria.

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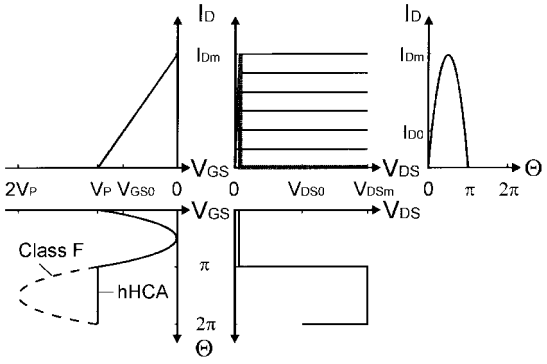

Fig. 1. Comparison of ideal waveforms and load lines of class F and hHCA.

TABLE I
COMPARISON OF ACHIEVEMENTS IN HIGH-EFFICIENCY POWER AMPLIFIER DESIGN REPORTED IN THE LITERATURE. REFERENCE (REF.), CLASS OF OPERATION (CLASS), FREQUENCY (f_0), OUTPUT POWER (P_{OUT}), POWER GAIN (G), DRAIN EFFICIENCY (η_D), AND POWER-ADDED EFFICIENCY (η_{PA}) ARE THE ABBREVIATIONS IN USE

Ref.	Class	f_0 [GHz]	P_{OUT} [dBm]	G [dB]	η_D [%]	η_{PA} [%]
[1]	F	1.75	24.5	11.0	77	71
[2]	F	0.9	35.7	12.7	56	53
[3]	F	0.84	32.0	-	76	-
[4]	F	1.7	31.8	11.8	73	68
[5]	F	0.9	33.0	11.0	76	70
[6]	E	1.0	29.7	14.7	75	73
[7]	rB	0.9	36.1	13.0	63	60
[8]	rB	0.8	36.2	12.2	66	62
[9]	HRA	2.0	37.0	12.0	75	70
[10]	HRA	1.7	34.1	9.0	86	75

II. Concept

Our amplifier concept is based on a modified class-A amplifier that uses a half-sinusoidal input signal to operate the transistor as a switch (see Fig. 1). With the suitable harmonic load—a short circuit at even harmonics and an open circuit at odd harmonics—the amplifier offers the same drain pulse forms and, therefore, the same drain efficiency as a class-F amplifier (ideally, 100%), but with the gain of class A. Consequently, power-added efficiency of this half-sinusoidally driven class-A harmonic-control amplifier (hHCA) is higher than that of class F. Due to a reduction of maximum negative gate voltage to half of the class-F value, the upper limit of the drain voltage, where gate-to-drain breakdown occurs, is higher for the new concept. Consequently, the drain bias voltage V_{DS0} can be increased, and this results in higher output power. Finally, reliability is expected to be improved too, as the gate of the device is stressed much less due to reduced input power and lower negative input voltage.

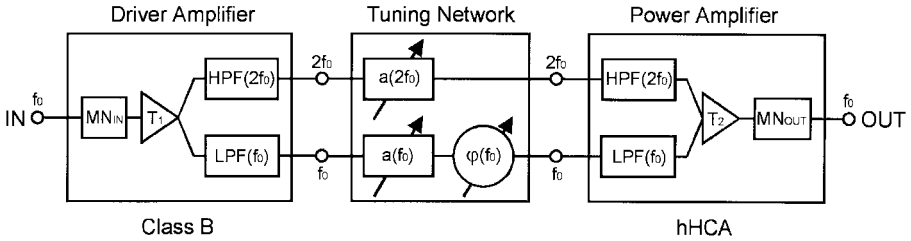

Fig. 2. Block diagram of the two-stage hHCA with external tuning network. Matching network: MN. High-pass filter: HPF. Low-pass filter: LPF. Transistor: T. Attenuator: a. Phase shifter: φ.

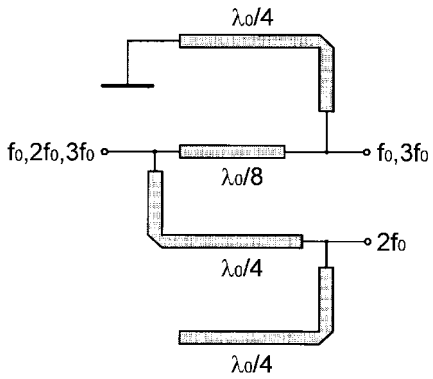

Fig. 3. Frequency diplexing network. Lengths of lines are given in wavelengths of fundamental frequency.

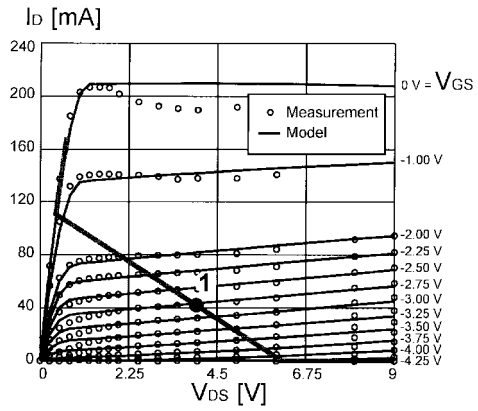

Fig. 4. Comparison of measured and modeled output dc characteristic and expected dynamic load line.

The desired input signal is generated by a pulse-shaping stage, which operates as a resistively loaded class-B amplifier, and needs to not be overdriven. This promotes the amplifier reliability too. As the drain current of the driver transistor is half sinusoidal too, intermodulation distortion of this amplifier stage is quite good. The high gain of the power stage keeps the reduction of overall efficiency due to the driver stage within a few percents, and this justifies the introduction of this two-stage hHCA concept.

III. Design

In Fig. 2, the block diagram of the two-stage amplifier is illustrated where the half-sinusoidal signal is approximated by the fundamental frequency along with the right portion of the second harmonic. At the driver FET output, the fundamental and second harmonic signal are separated from each other by an appropriate filtering network. With two continuously variable attenuators and a continuously variable phase shifter $[\varphi(f_0) = 0, \cdots, 180°]$, the optimum input signal can be adjusted at the gate of the power FET after combining both signal paths. When magnitude and phase relation of both input signals of the power amplifier are known, the bias point of the driver amplifier is changed for this optimum fundamental and second harmonic output power and the interstage tuning network is replaced by a hybrid phase shifter, which can be simply integrated in the fundamental frequency path.

In order to separate/combine fundamental and second harmonic-frequency signal, we constructed a frequency diplexing network, as illustrated in Fig. 3. Lengths of lines are indicated in wavelengths of fundamental frequency. At the fundamental frequency output, a short-circuit stub of one quarter-wavelength is used to achieve a short at the second harmonic and an open at the fundamental frequency. This open at the fundamental frequency does not influence the behavior of the circuit at the fundamental frequency, but the short at the second harmonic is transformed by a one-eighth wavelength line to an open at the input. At the second harmonic output, an open circuit stub of one quarter-wavelength is used to achieve a short at the fundamental frequency and an open at the second harmonic. This short at the fundamental frequency is transformed by a quarter-wave transformer to an open at the input. A more detailed analysis of this circuit shows that all odd harmonics are guided to the fundamental frequency output, whereas all even harmonics are guided to the output of the second harmonic. Based on this circuit, we were able to control the impedance matching of the first three harmonics at the driver-amplifier output and the power-amplifier input independently.

We used commercially available packaged GaAs FET's for the development of a hybrid version of driver and power stage of an hHCA at 1.62 GHz. For our simulations with a harmonic-balance simulation software,[1] we generated large-signal models of various FET's with a commercially available transistor parameter extraction software.[2] Therefore, we performed device dc and multiple-bias small-signal S-parameter measurements.

A modified TriQuint's Own model [13] was selected for modeling of our devices, as it describes the soft pinchoff

[1] Hewlett-Packard, JOmega, Series 4, Version 5, HP-EEsof, Santa Rosa, CA, Feb. 1994.

[2] OSA, HarPE, Version 1.8, Optimization Systems Associates Inc., Dundas, Ont., Canada L9H 5E7.

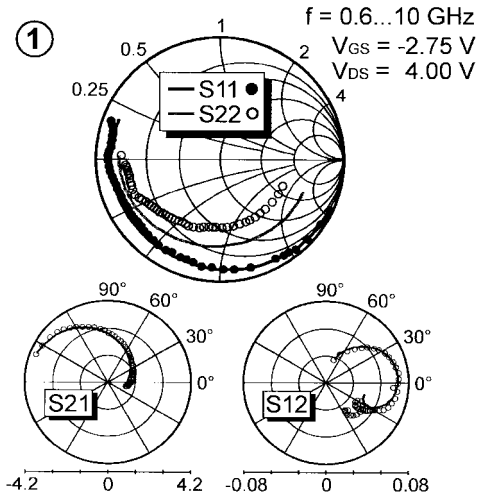

Fig. 5. Comparison of measured and modeled S-parameters at bias-point 1.

and the transition from ohmic-to-saturation region most realistically for our purpose. Fig. 4 compares measured (circles) and modeled (lines) output dc characteristics of a medium-power GaAs FET with the expected dynamic load line for use within a high-efficiency amplifier. In Fig. 5, small-signal S-parameters at a typical bias point in saturation on this dynamic load line are illustrated. We could achieve excellent agreement of measured and modeled dc characteristics and S-parameters even in the ohmic region and at pinchoff.

Using these transistor models, we performed extensive circuit simulations, which resulted in the selection of the most appropriate device. The most promising results were achieved with a device of Thomson. In Fig. 6, the simulated pulse forms at inner gate and inner drain of the hHCA power device are indicated. As expected from theory, the gate voltage is half sinusoidal, the drain current is half sinusoidal too, and the drain voltage is more or less rectangular. The marked voltage and current ripple during the second half of the period, where the device is pinched off, results from resonant effects caused by the transistor housing. The simulated performance of the hHCA power stage at 1.62 GHz was 79% drain efficiency at 15-dB power gain, which corresponds with a power-added efficiency of 76%. The required fundamental to second harmonic input power ratio was 7.8 dB (see Table II).

In Fig. 7, the layout of the half-sinusoidally driven power stage is shown. Several tuning possibilities were foreseen within the matching networks (MN's) to fine tune its performance. Stubs 1 and 2 provide the fundamental frequency-input matching. As these stubs are connected via a quarter-wave transformer, it is possible to adjust magnitude and phase of the fundamental frequency-source reflection coefficient $\Gamma_S(f_0)$ independently. In Fig. 8(a), it is illustrated that a variation of the length l_1 of stub 1 only influences the magnitude of $\Gamma_S(f_0)$, whereas second and third harmonic-source reflection coefficients remain unchanged. Similarly, variations of the length l_2 of stub 2 only changes the phase of $\Gamma_S(f_0)$, as shown in Fig. 8(b). In the same way, second harmonic input matching was performed with stubs 3 and 4. At the output, we implemented tuneable stubs to control the phases of

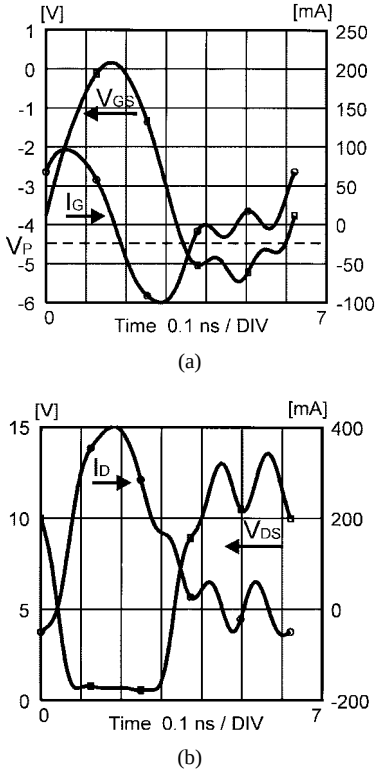

Fig. 6. Simulated signal pulse forms at (a) inner gate and (b) inner drain of half-sinusoidally driven power amplifier at optimum bias point at 1.62 GHz. V_P indicates the pinchoff voltage.

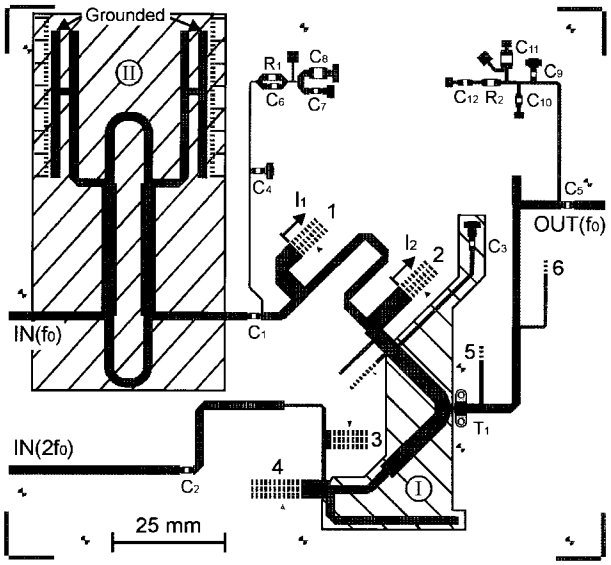

Fig. 7. Layout of final hHCA power stage. Tuning stubs (1–6), the frequency diplexing network (I), and the hybrid phase shifter (II) are identified.

second (stub 6) and third harmonic-load reflection coefficients (stub 5), which were crucial for an optimum drain pulse shaping and, therefore, for maximum power-added efficiency.

Additionally, the frequency diplexing network (I) and the hybrid phase shifter (II) are indicated in Fig. 7. The hybrid variable phase shifter, which is used to adjust the optimum phase relation between fundamental frequency and second harmonic input signals, was implemented at the fundamental

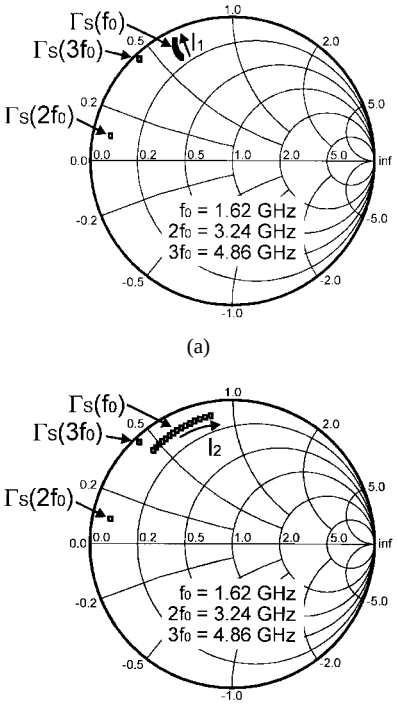

Fig. 8. Simulated fundamental frequency, second, and third harmonic-source reflection coefficients of input MN of hHCA power stage as a function of (a) length l_1 of stub 1 and (b) length l_2 of stub 2.

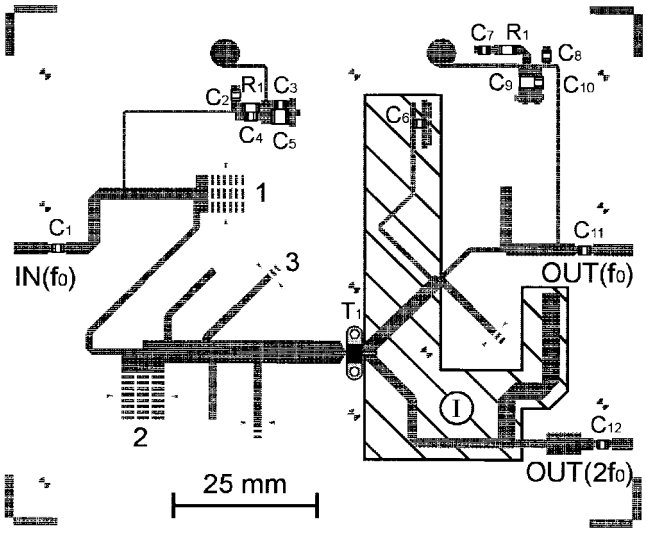

Fig. 9. Layout of pulse forming driver stage. Tuning stubs (1–3) and the frequency diplexing network (I) are identified.

frequency-input port of the final hHCA power stage. It is based on a quadrature hybrid with through and coupled ports connected with two short-circuited transmission lines with the same length. The whole power appears at the isolated port with a phase difference to the input signal proportional to twice the length of these lines. To vary the phase angle of fundamental frequency-input signal between 0°–180°, quarter-wave-long transmission lines with variable shorts were needed.

The layout of the pulse-forming driver amplifier is indicated in Fig. 9. Again, magnitude and phase of fundamental frequency-input reflection coefficient could be adjusted independently using stubs 1 and 2, respectively. Furthermore, a tuning stub for the phase of second harmonic-source impedance matching (stub 3) was foreseen to adjust the amplifiers' fundamental to second harmonic output power ratio. At the driver-stage output, the frequency diplexing network (I) was optimized for signal separation and, afterwards, output MN's for the fundamental frequency and the second harmonic-frequency output path were optimized independently too.

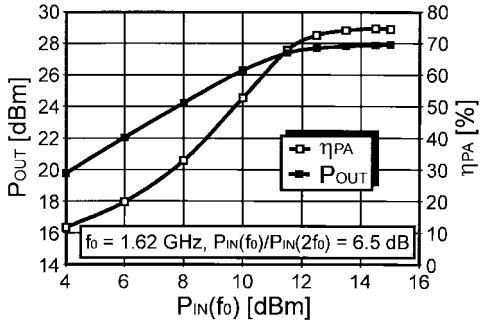

Fig. 10. Measured output power and power-added efficiency versus fundamental input power of half-sinusoidally driven power amplifier at 1.62 GHz and $P_{\mathrm{IN}}(f_0)/P_{\mathrm{IN}}(2f_0) = 6.5$ dB.

TABLE II
COMPARISON OF SIMULATION AND MEASUREMENT OF hHCA AND CLASS-F POWER AMPLIFIER AT 1.62 GHz

Power Amplifier	POUT [dBm]	G [dB]	ηD [%]	ηPA [%]	PIN(f0)/PIN(2f0) [dB]
hHCA (Simulation)	28.2	15.1	79	76	7.8
hHCA (Measurement)	27.9	14.4	77	74	6.5
Class F (Measurement)	26.8	11.4	77	71	-

IV. PERFORMANCE

The first realizations of driver and power amplifier on a Teflon substrate with $\varepsilon_r = 2.5$ and 0.762-mm height operated optimally with only little tuning at the specified stubs. Therefore, no redesigns had to be performed, and the amplifier could be fully designed with the circuit simulator at the first run.

Measured output power and power-added efficiency characteristics over fundamental frequency-input power of the half-sinusoidally driven power-amplifier stage are shown in Fig. 10. This measurement was performed at center frequency (1.62 GHz) at constant drain-to-source bias voltage and drain bias current of 6.1 V and 130 mA, respectively. Fundamental-to-second harmonic input power ratio was held constant at 6.5 dB. At optimum input power, the power amplifier delivers 77% drain efficiency, 74% power-added efficiency, 27.9-dBm output power, and 14.4-dB gain. This is in good agreement with the simulated performance (see Table II). In comparison with a power stage with the same FET operated at class F, we can achieve, with our amplifier concept, 1.1 dB higher output power and 3 dB higher gain at the same drain efficiency, which results in a 3% higher power-added efficiency.

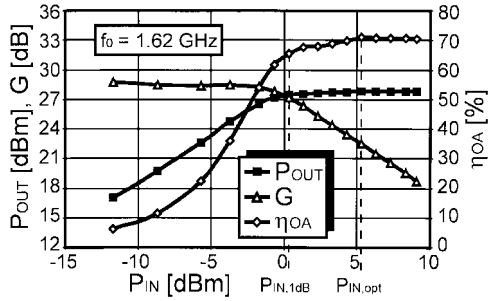

Fig. 11. Measured output power, gain, and overall efficiency versus input power of two-stage hHCA at 1.62 GHz.

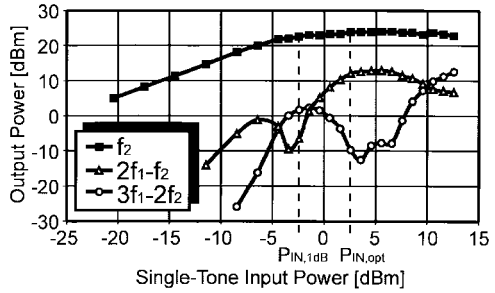

Fig. 12. Measured two-tone characteristics—single-tone output power, third- and fifth-order intermodulation products—versus single-tone input power of two-stage hHCA at $f_1 = 1.615$ GHz and $f_2 = 1.62$ GHz.

TABLE III
MEASURED SC AND TWO-TONE PERFORMANCE OF TWO-STAGE hHCA AND OF DRIVER STAGE, RESPECTIVELY, AT $f_1 = 1.615$ GHz AND $f_2 = 1.62$ GHz

	$P_{OUT,SC}$ [dBm]	$\eta_{OA,SC}$ [%]	G_{SC} [dB]	IMD_3 [dBc]	IMD_5 [dBc]	$IMD_{3,D}$ [dBc]	$IMD_{5,D}$ [dBc]
$P_{IN,opt}$	27.9	71	22.4	-12	-33	-15	-20
$P_{IN,1dB}$	27.4	64	27.2	-29	-21	-28	-23

In Fig. 11, the performance of the combination of driver and power amplifier with integrated interstage tuning network is illustrated as a function of input power. The driver stage was biased at constant drain to source voltage of 2.3 V and constant gate to source voltage of −4.45 V. At optimum input power, the two-stage amplifier delivers 71% overall efficiency, 27.9-dBm output power, and 22.4-dB gain (see Table III) at a voltage standing-wave ratio at its input of 1.5. At this point, the amplifier is almost 6 dB in gain compression. Levels of second and third harmonics at the output of the power stage are measured at −24 and −30 dBc, respectively. Within a 40-MHz bandwidth from 1.60 to 1.64 GHz, overall efficiency is larger than 67%.

Two-tone measurements were performed on the two-stage amplifier to determine its distortion characteristics (see Fig. 12 and Table III). At optimum input power, third-order intermodulation distortion is 12 dB below the carrier. At 1-dB gain compression, where the amplifiers' single-carrier (SC) overall efficiency is still 64%, third-order intermodulation products lie 29 dB below the carrier. At this input power level, fifth-order intermodulation is (with −21 dBc) the predominating distortion.

It should be noted that our amplifier was not optimized for low distortion, but for high-efficiency characteristics and, therefore, seems to be capable of improvement in the light of the former without degrading the latter. Inspecting the two-tone measurement results, we can draw two important conclusions. On the one hand, it is remarkable that fifth-order intermodulation distortion is larger than third-order intermodulation distortion. At the fundamental frequency output of the driver-amplifier stage, levels of fourth- (−25 dBc) and fifth-order harmonics (−35 dBc) are larger than second- (−38 dBc) and third-order harmonics (−43 dBc). In both amplifier stages, harmonics have been terminated specifically only up to the third-order, whereas transistors' transit frequencies are high enough to offer high gain at even higher harmonics. It can be expected that a control of higher order harmonics up to the fifth will lead to a marked improvement of fifth-order intermodulation distortion. On the other hand, a comparison of intermodulation characteristics of driver amplifier ($IMD_{3,D}$, $IMD_{5,D}$) and two-stage amplifier at 1-dB gain compression shows that the driver stage is primarily responsible for nonlinear distortion (see Table III). Therefore, a further improvement of amplifier linearity must first of all start at its driver stage.

V. SUMMARY

The hHCA is an innovative high-efficiency harmonic-control amplifier concept where the power stage is driven by a half-sinusoidal signal, which is generated by a resistively loaded class-B amplifier. The power stage delivers high power-added efficiency along with class-A gain. The realization of such a two-stage hHCA at 1.62 GHz has demonstrated 71% overall efficiency, 27.9-dBm output power, and 22.4-dB gain. Intermodulation distortion of this amplifier is low even in saturation where its overall efficiency is high.

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Bernhard Ingruber (S'98) received the Dipl.-Ing. degree in electrical engineering from Vienna University of Technology, Vienna, Austria, in 1992, and is currently working toward the Ph.D. degree.

Following graduation, he was with the Austrian Research Center Seibersdorf, where he was engaged in a comparative study of existing safety standards of human exposure to microwave radiation. Since 1994, he has been a Research Assistant in the Department of Communications and Radio-Frequency Engineering, Vienna University of Technology, where he is involved in the analysis, design, and testing of high-efficiency and high-linearity microwave power amplifiers for hand-held terminals for mobile communication systems.

Werner Pritzl (S'95–A'95) was born in Lustenau, Austria, in 1962. He received the Dipl.-Ing. degree in electrical engineering/communication engineering and the Dr.Techn. degree (with honors) from Vienna University of Technology, Vienna, Austria, in 1987 and 1995, respectively.

From 1988 to 1995, he was a Research Assistant at the Department of Communications and Radio-Frequency Engineering, Vienna University of Technology. His research activities involving remote sensing of weather-induced road condition and high-efficiency power amplifiers. In 1995, he joined the R&D Department, ERNE Fittings GmbH & Co. Since 1997, he has been with the R&D Department, ELB-Form GmbH, Vienna, Austria.

Dr. Pritzl received the Holzer Award for new ideas and developments with technical applicability in 1995.

Dieter Smely received the Dipl.-Ing degree in electrical engineering from Vienna University of Technology, Vienna, Austria, in 1997, and is currently working toward the Ph.D. degree.

He joined the Department of Communications and Radio-Frequency Engineering, Vienna University of Technology in 1996, where he is currently a Research Assistant. He is responsible for the design of high-precision microwave test fixtures and computer-controlled microwave measurements. In addition, he specializes in GaAs MESFET models. He is currently engaged in the development of high-power solid-state amplifiers.

Martin Wachutka (S'92) was born in Opponitz, Austria, on September 15, 1970. He received the Dipl.-Ing. degree in electrical engineering from Vienna University of Technology, Vienna, Austria, in 1996.

In 1996, he joined the Department of Communications and Radio-Frequency Engineering, Vienna University of Technology, as a Research Assistant. He is currently working in the field of high-efficiency high-power amplifiers.

Gottfried Magerl (M'78) was born in Vienna, Austria, on August 16, 1947. He received the Dipl.-Ing. and Dr.Techn. degree from the Vienna University of Technology, Vienna, Austria, in 1972 and 1975, respectively.

Since 1973, he has been with the Institute of Communications and Radio Frequency Engineering, Vienna University of Technology. In 1981, he was appointed Academic Lecturer (Universitätsdozent). In 1990, he became University Professor of Microwave Engineering, and he recently became Head of the Institute of Electronic Design and Measurement Techniques. He spent the 1981–1982 academic year and the summer months of 1984 and 1986 at the University of Chicago and the University of Michigan, East Lansing, where he constructed high-resolution IR spectrometers based on the microwave modulation of CO_2 and CO lasers via the electrooptic effect in CdTe. His interest in the application of electromagnetic radiation to noncontacting measurement techniques lead to the development of a road-condition sensing microwave radar and to extensive work on physics and optimization of narrow-band atomic line filters. His current research interests concentrate on the development of highly efficient linear microwave power amplifiers for mobile communications.